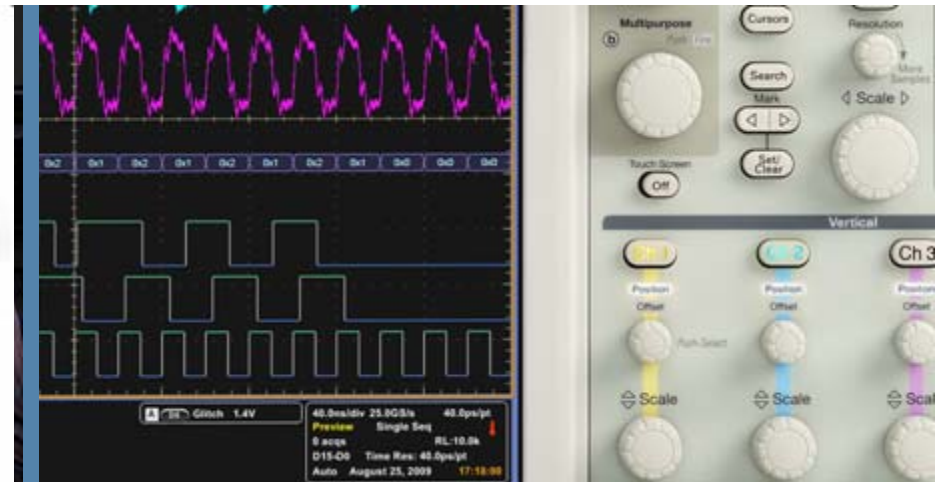
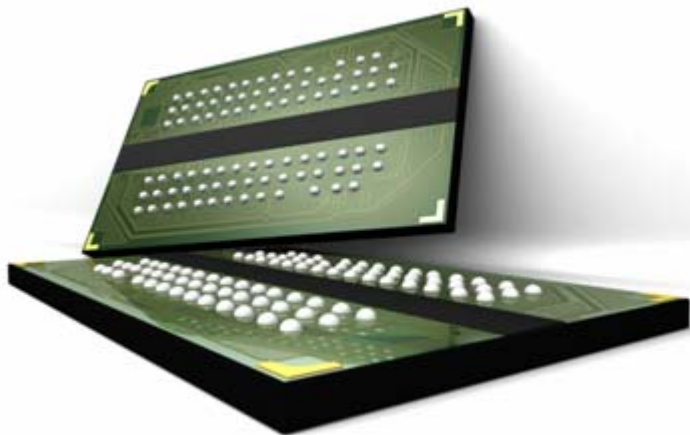
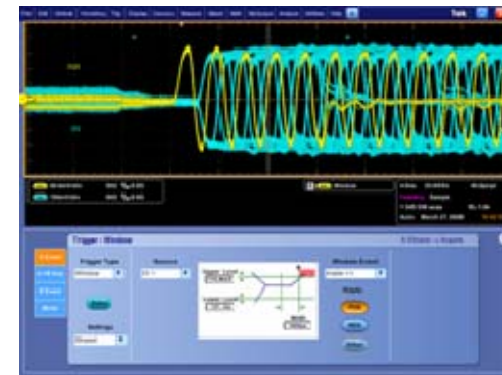


DDR Verification Approaches



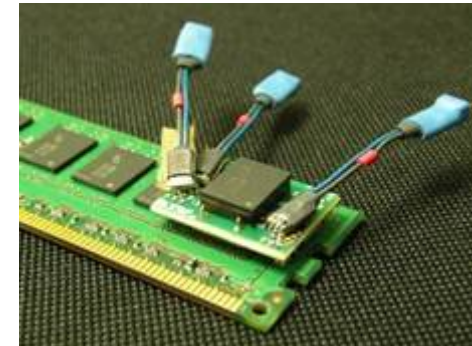
DDR Test Challenges

- Signal Access & Probing
 - Easy-to-use / reliable connections
 - Bandwidth & Signal Integrity
 - Affordable
- Isolation of Read/Write bursts
 - Triggering or Post-Processing (ASM)
- Complexity of JEDEC Conformance Tests
 - V_{ref} / V_{ih} / V_{il}
 - Derating
- Results Validity / Statistics
- Effective Reporting / Archiving
- Advanced Analysis
 - Characterization
 - Debug

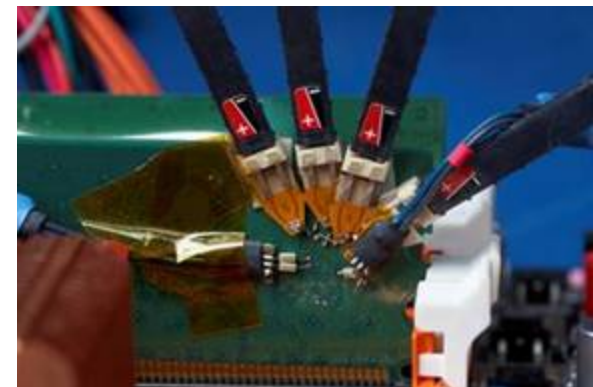


Challenge 1: Probing DDR Memory

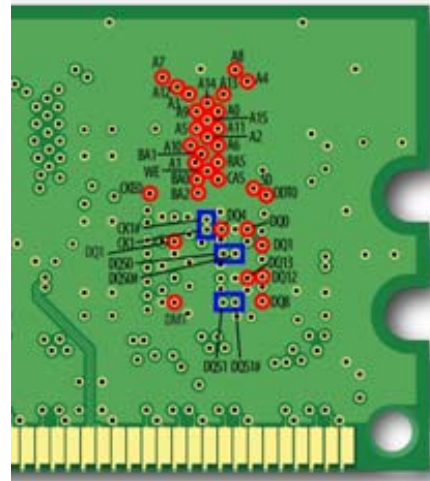
- Computer Systems use standardized DIMM's for which several probing solutions are available
- Memory in Embedded Designs is usually directly mounted on the PCB
- All DDR2 & DDR3 Components use BGA Packages
- Probing a BGA package is Difficult
 - Unable to probe at the Balls of the Device
- Signal Access Solutions
 - Component Interposers
 - Direct Probing
 - Analog Probing
 - DQ, DQS, Clock
 - Digital Probing
 - Address
 - Command
 - Power, Reset, and Reference



Component Interposer

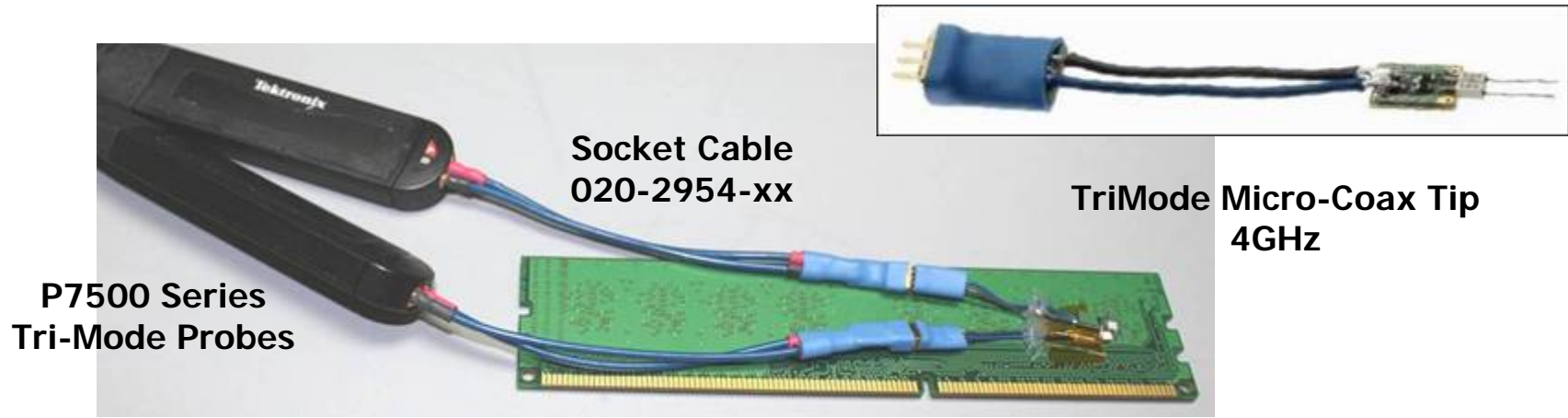


Analog and Digital Probing



Direct Probing

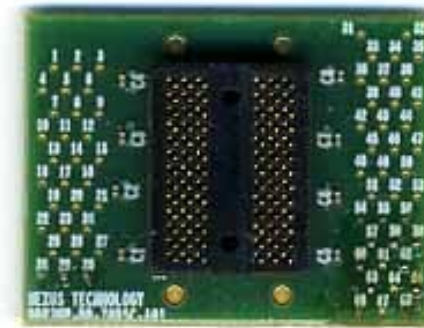
Analog Solder-In Probing Solutions for DDR



Nexus DDR3 BGA Chip Interposers For Oscilloscopes



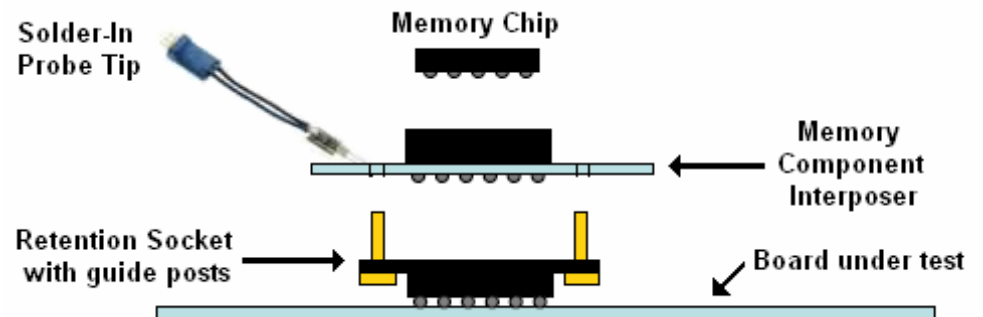
Retention Socket



BGA Chip Interposer

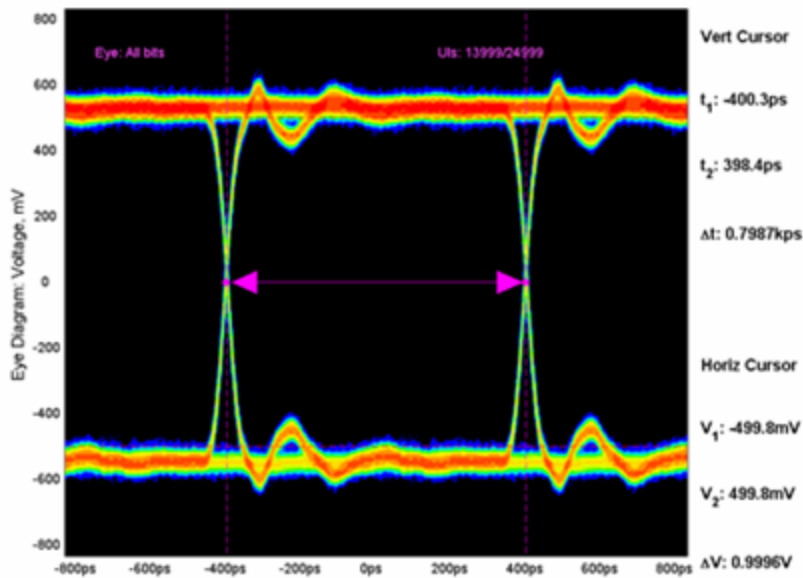
BGA Chip Access For DDR2, DDR3

- Unique, reusable socket design allows for multiple chip exchanges
- Able to use both analog and digital probes
- Nexus DDR Interposers sold by Tektronix
 - DDR2 and DDR3 versions
 - X4/x8, x16 pins
 - Socket and solder models (See MSR for details)

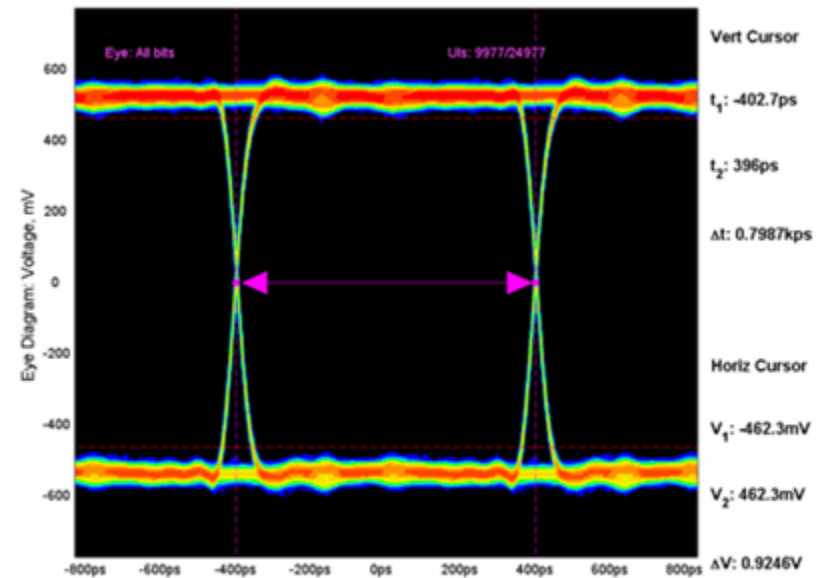


BGA Chip Interposer – Signal Fidelity

- Filters are available to de-embed analog effects
 - Library of filters is provided with the interposer
 - Filters were developed based on the actual S-parameters of the interposer + probe tip
 - Available for DPO/DSA/MSO70000 and DPO7000 scopes



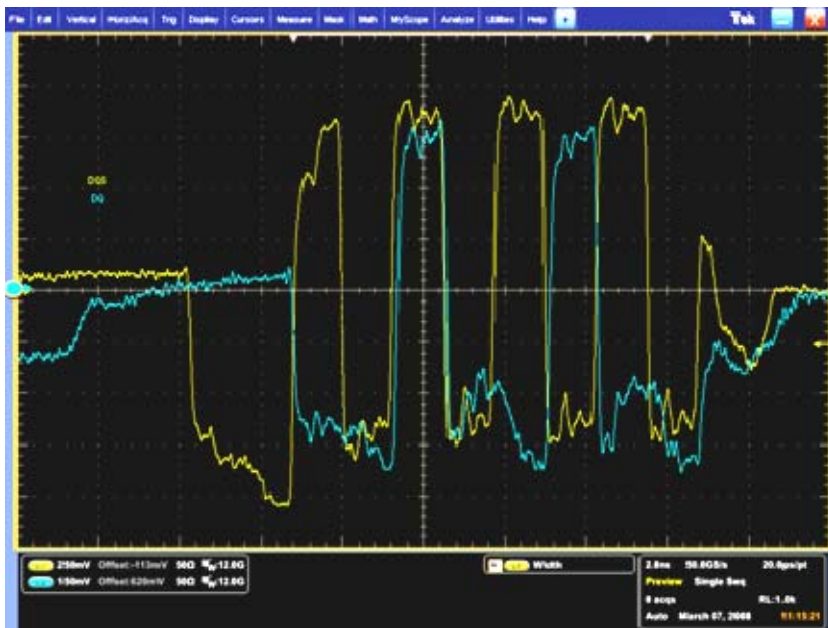
Eye - unfiltered



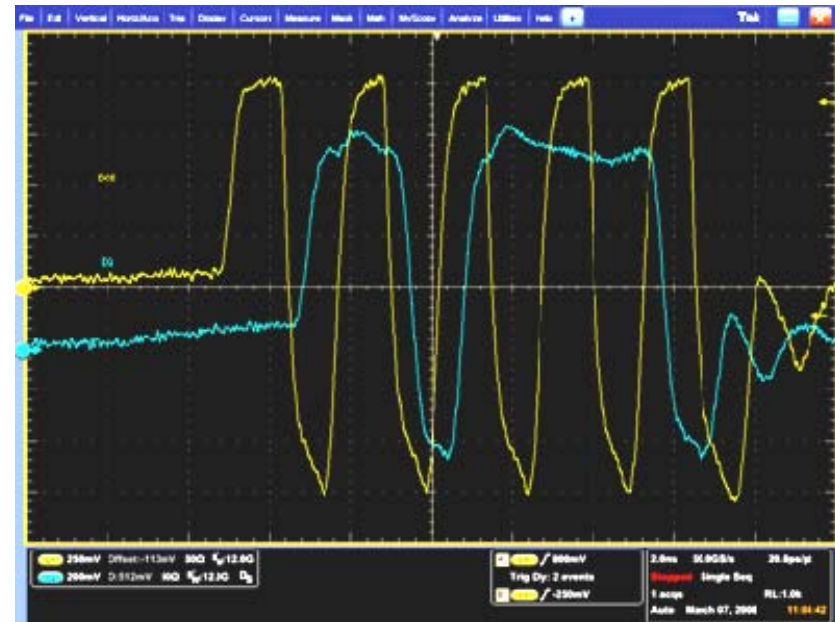
Eye – with filter

Challenge 2: Burst Identification

- Locate the right kind of bursts (read vs write)
- Locate the precise edges of each burst
- Refine burst identity based on other criteria (rank, secondary bus state, etc)



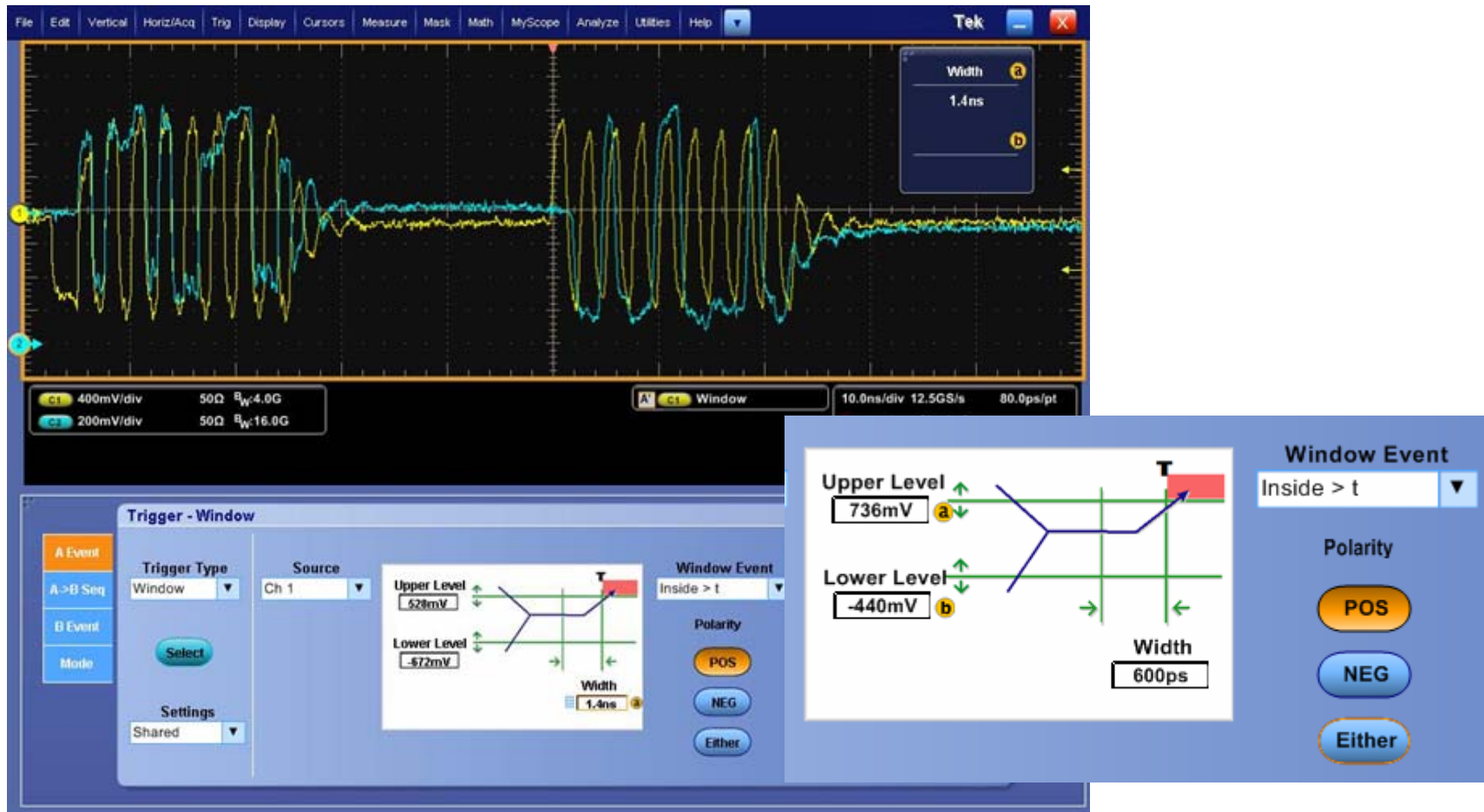
DDR3 Read Burst



DDR3 Write Burst

HW Triggering on DDR Reads / Writes

- Window Trigger - useful for real-time DDR read /write isolation
 - DQS goes high for writes, low for reads (DDR3)



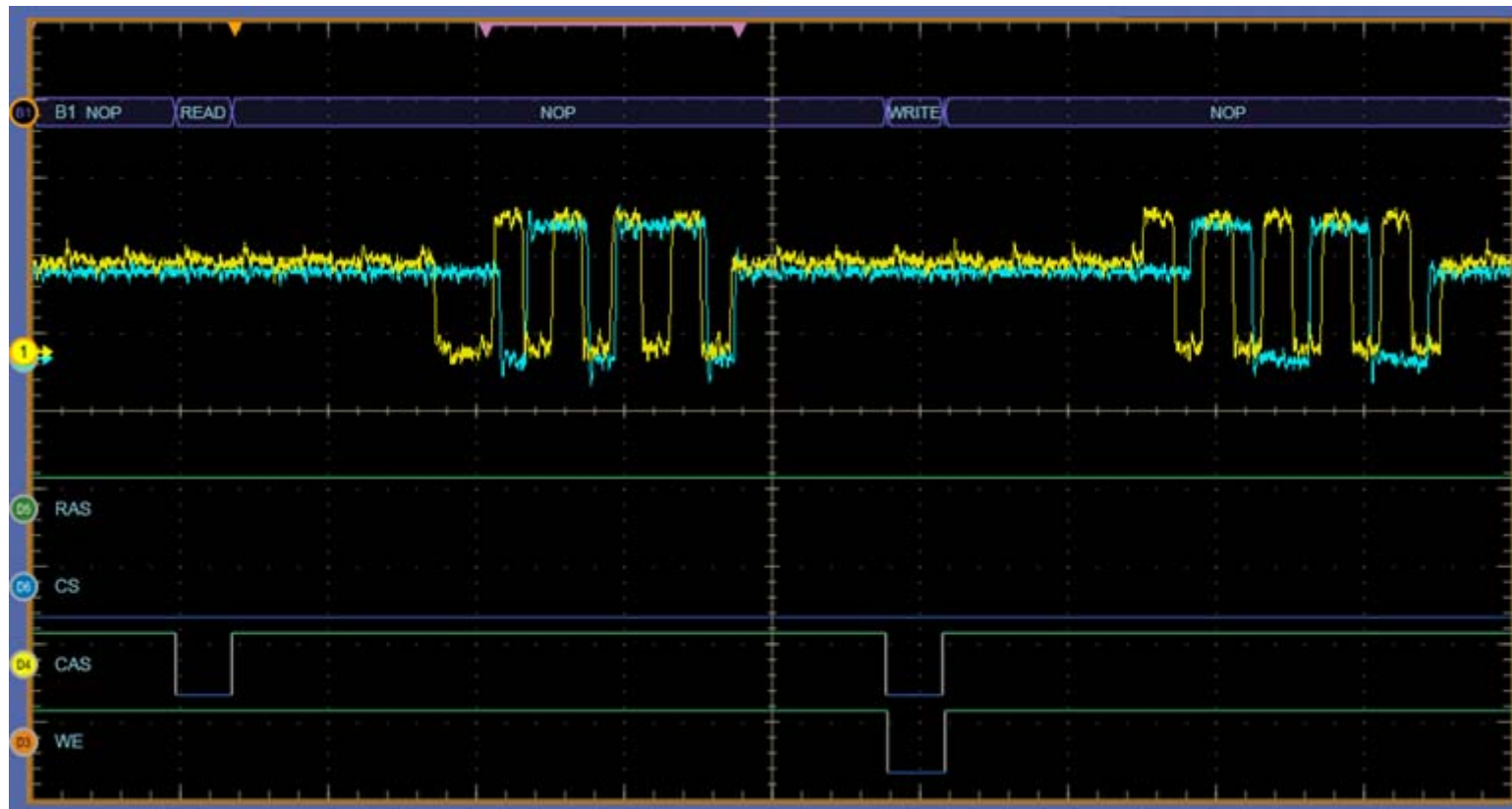
Advanced Search & Mark (ASM) and Long Records

- Easily identify & measure all Read / Write bursts in the acquisition
 - Based on the Advanced Search & Mark feature
 - Scroll through marked reads / writes across the entire waveform record



Burst Identification on an MSO

- Using bus state, specific transactions can be isolated
 - For example, locate only Reads from a specific memory rank
 - Advanced Search & Mark is used for fine burst positioning



Challenge 3: Measurement Setup

- JEDEC Standards specify measurements & methods

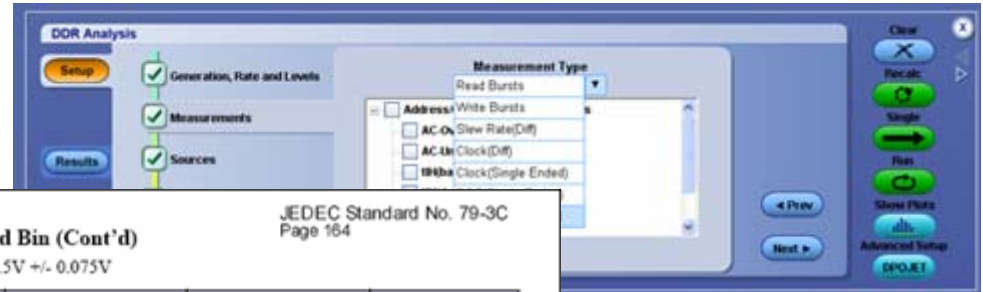


Table 65 — Timing Parameters by Speed Bin (Cont'd)

JEDEC Standard No. 79-3C
Page 164

NOTE: The following general notes from page 170 apply to Table 65: Note a. VDD = VDDQ = 1.5V +/- 0.075V

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units	Notes
		Min	Max	Min	Max	Min	Max	Min	Max		
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	-193	193	-169	169	ps	
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	-200	200	-175	175	ps	
Cumulative error across 10 cycles	tERR(10per)	-257	257	-231	231	-205	205	-180	180	ps	
Cumulative error across 11 cycles	tERR(11per)	-263	263	-237	237	-210	210	-184	184	ps	
Cumulative error across 12 cycles	tERR(12per)	-269	269	-242	242	-215	215	-188	188	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	$tERR(nper)_{min} = (1 + 0.68 \ln(n)) * tJIT(per)_{min}$ $tERR(nper)_{max} = (1 + 0.68 \ln(n)) * tJIT(per)_{max}$								ps	24
Data Timing											
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps	13
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)	13, g
DQ low-impedance time from CK, CK#	tLZ(DQ)	-800	400	-600	300	-500	250	-450	225	ps	13, 14, f
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps	13, 14, f
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)	75	-	25	-	30	-	10	-	ps	d, 17
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)	150	-	-	-	-	-	-	-	-	-
DQ and DM Input pulse width for each input	tDIPW	600	-	-	-	-	-	-	-	-	-
Data Strobe Timing											
DQS, DQS# differential READ Preamble	tRPRE	0.9	Note 13	-	-	-	-	-	-	-	-
DQS, DQS# differential READ Postamble	tRPST	0.3	Note 13	-	-	-	-	-	-	-	-
DQS, DQS# differential output high time	tQSH	0.38	-	-	-	-	-	-	-	-	-
DQS, DQS# differential output low time	tQSL	0.38	-	-	-	-	-	-	-	-	-
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	-	-	-	-	-	-	-	-
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	-	-	-	-	-	-	-	-
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-400	400	-	-	-	-	-	-	-	-

8.1 AC and DC Logic Input Levels for Single-Ended Signals

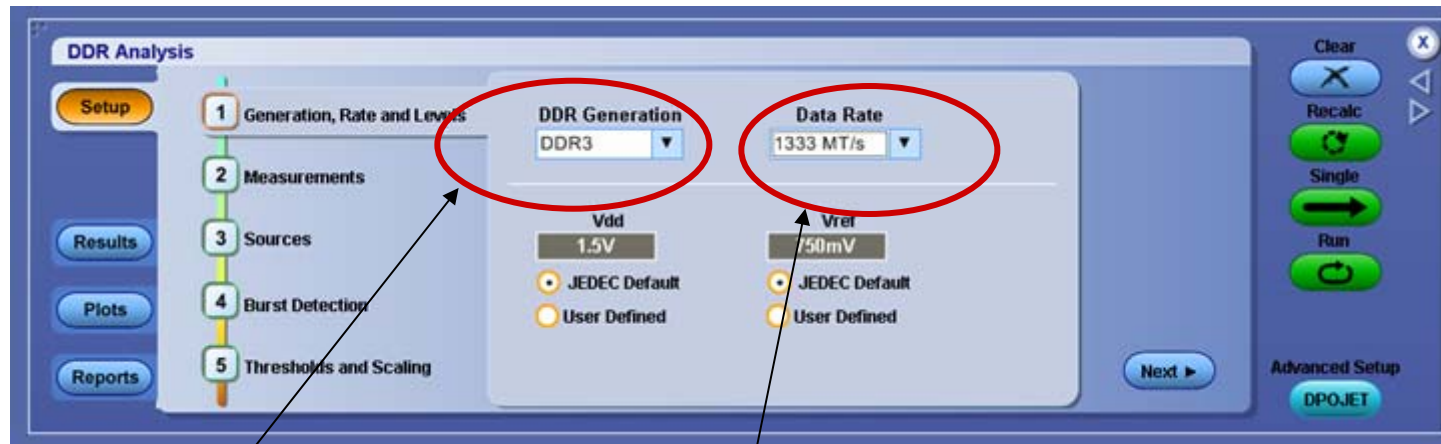
8.1.1 AC and DC Input Levels for Single-Ended Command and Address Signals

Table 24 — Single-Ended AC and DC Input Levels for Command and Address

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit	Notes
		Min	Max		
V _{IH,CA} (DC)	DC input logic high	V _{ref} + 0.100	VDD	V	1
V _{IL,CA} (DC)	DC input logic low	VSS	V _{ref} - 0.100	V	1
V _{IH,CA} (AC)	AC input logic high	V _{ref} + 0.175	Note 2	V	1, 2
V _{IL,CA} (AC)	AC input logic low	Note 2	V _{ref} - 0.175	V	1, 2
V _{IH,CA} (AC150)	AC input logic high	V _{ref} + 0.150	Note 2	V	1, 2
V _{IL,CA} (AC150)	AC input logic low	Note 2	V _{ref} - 0.150	V	1, 2
V _{RefCA} (DC)	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V	3, 4

Ease of Use - DDRA Wizard

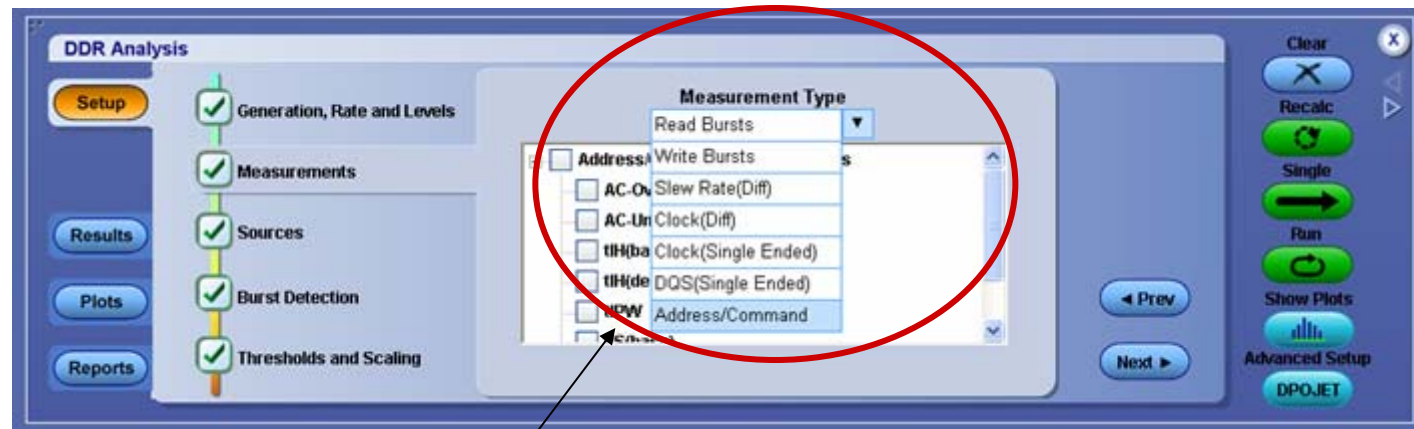
Step #1



Select DDR Generation

Select DDR Rate

Step #2



Choose measurements (Read / Write / CLK / Addr & Command)

Comprehensive Measurement Support

Option DDRA supports a broad range of JEDEC-specified measurements for DDR, DDR2, DDR3, LP-DDR

► Example measurements list for DDR2 :

- tCK(avg)
- tCK(abs)
- tCH(avg)
- tCH(abs)
- tCL(avg)
- tCL(abs)
- tHP
- tJIT(duty)
- tJIT(per)
- tJIT(cc)
- tERR(02)
- tERR(03)
- tERR(04)
- tERR(05)
- tERR(6 - 10 per)
- tERR(11 - 50 per)
- tDQSH
- tDS - diff (base)
- tDS - SE (base)
- tDS -diff - DERATED
- tDS -SE - DERATED
- tDH - diff (base)
- tDH - SE (base)
- tDH -diff - DERATED
- tDH -SE - DERATED
- tDIPW
- tAC - diff
- tDQSCK -diff
- tDQSCK - SE
- tDQSQ - diff
- tDQSQ - SE
- tQH
- tDQSS
- tDSS
- tDSH
- tIPW
- tIS (base)
- tIH (base)
- tIS - DERATED
- tIH - DERATED
- Vid - diff (AC)
- Vix (AC) - DQS
- Vix (AC) - CLK
- Vox (AC) - DQS
- Vox (AC) - CLK
- Input Slew-Rise (DQS),
- Input Slew-Fall (DQS),
- Input Slew-Rise (CLK),
- Input Slew-Fall (CLK),
- AC - Overshoot Amplitude - diff
- AC -Undershoot Amplitude - diff
- AC - Overshoot Amplitude - SE
- AC - Undershoot Amplitude - SE
- Data Eye Width

Measurement De-rating

- JEDEC stipulates de-rating of DDR2 and DDR3 pass / fail limits for Setup & Hold measurements based on signal slew rate*
- Option DDRA automatically calculates slew rates and applies the appropriate de-rating values to the measurement limits.

- tDS - diff (base)
- tDS -diff - DERATED
- tDS - SE (base)
- tDS -SE - DERATED
- tDH - diff (base)
- tDH -diff - DERATED
- tDH - SE (base)
- tDH -SE - DERATED
- tIS (base)
- tIS - DERATED
- tIH (base)
- tIH - DERATED

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Page 176

13 Electrical Characteristics and AC Timing (Cont'd)
13.3 Address / Command Setup, Hold and Derating (Cont'd)

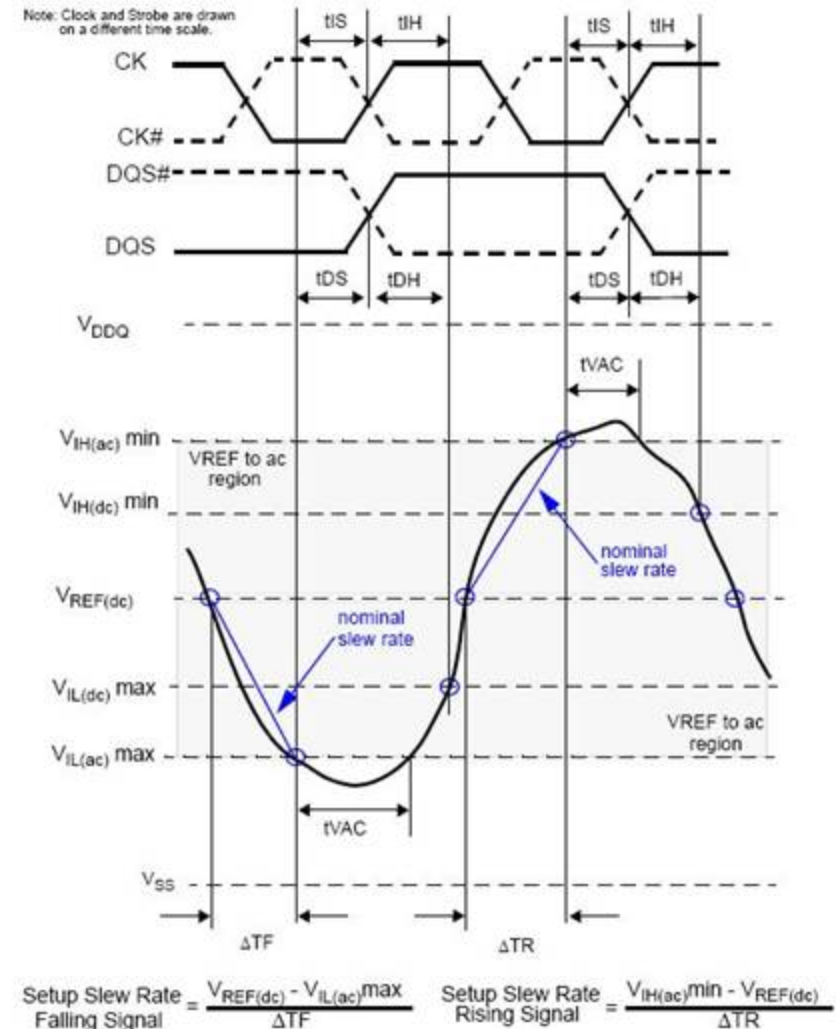
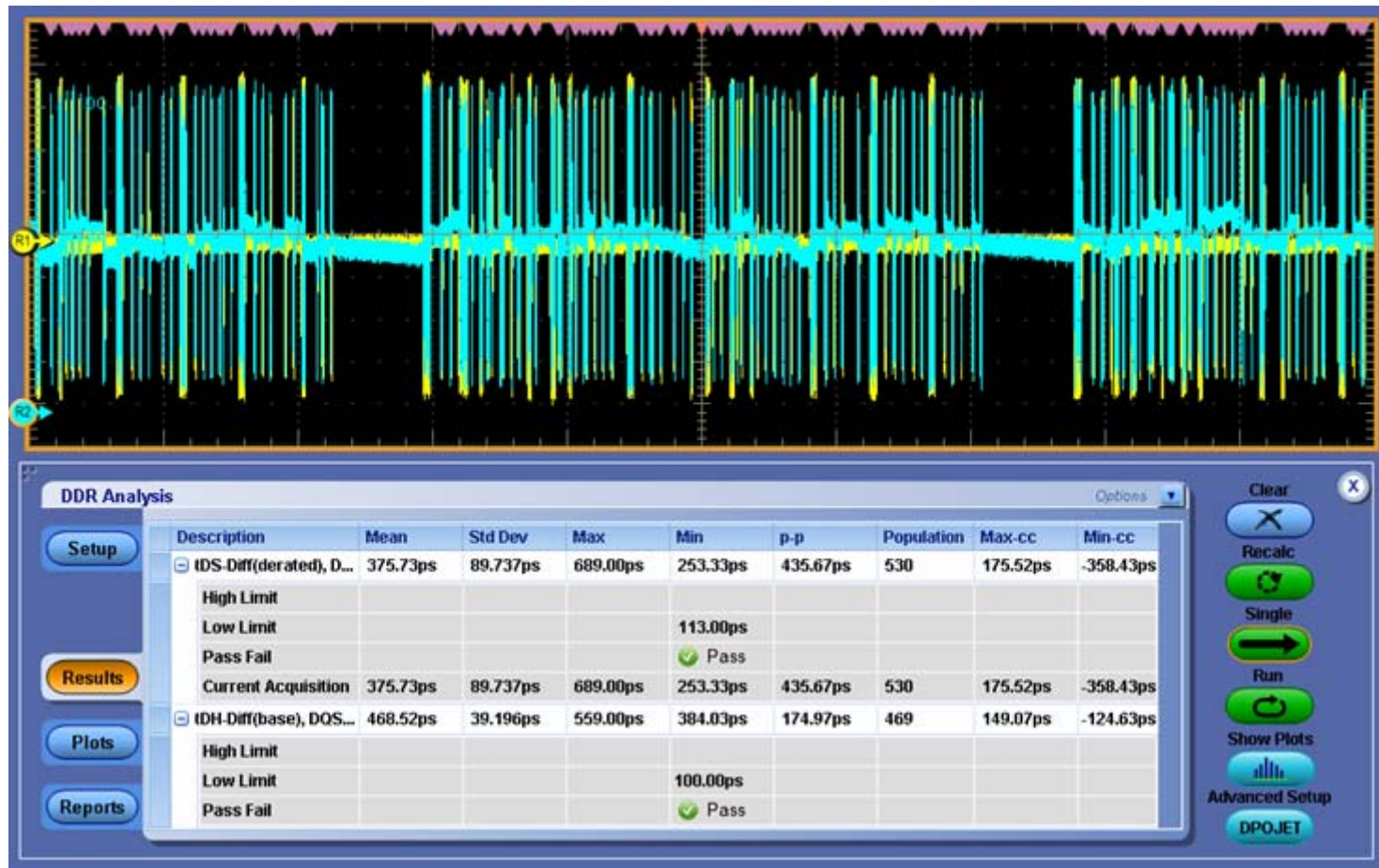


Figure 110 — Illustration of nominal slew rate and t_{VAC} for setup time t_{DS} (for DQ with respect to strobe) and t_{IS} (for ADD/CMD with respect to clock).

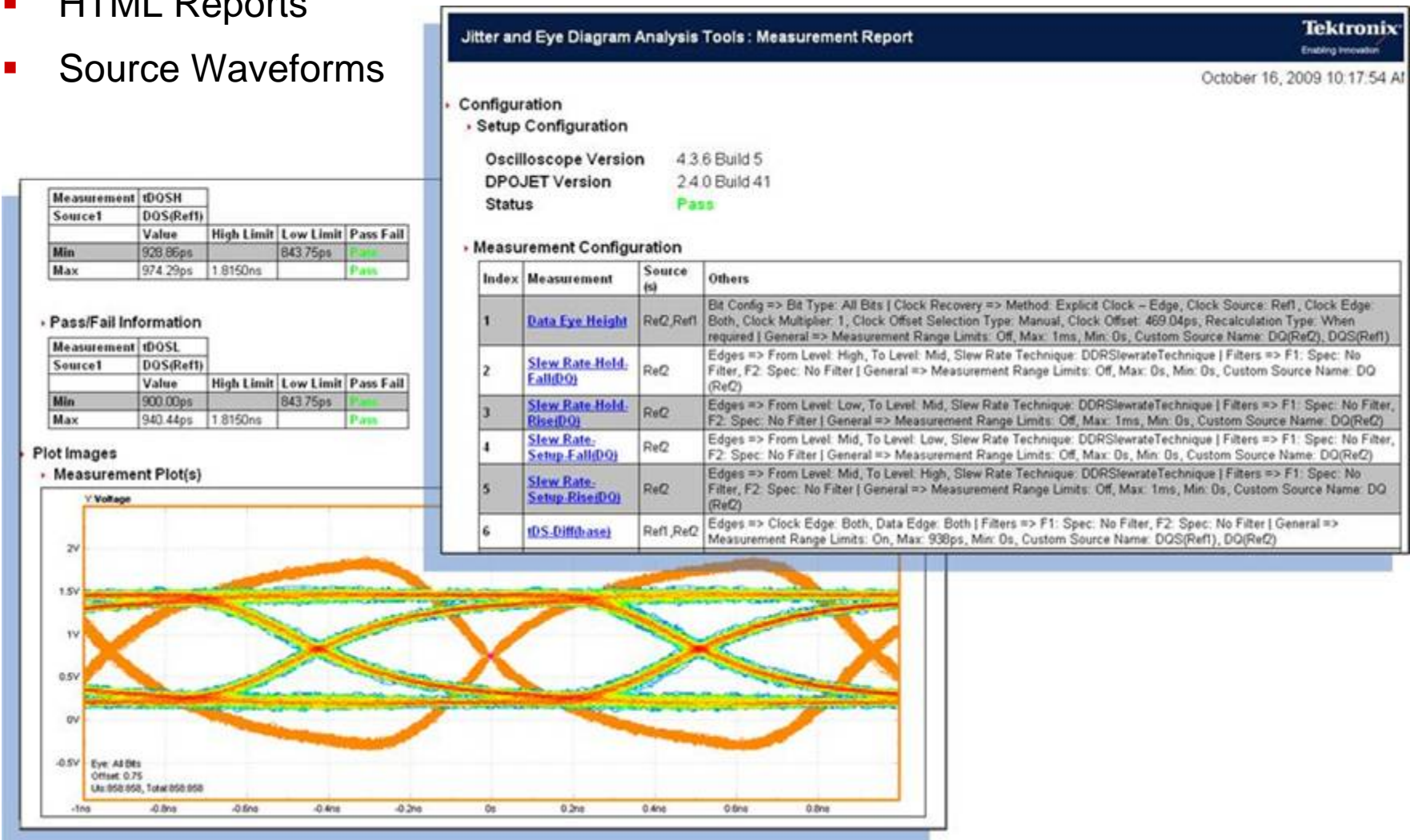
Challenge 4: Results and Statistical Validity

- To have confidence in your test results, you need 100's, 1000's or even more observations of each measurement
- As a practical matter, measurement throughput is essential



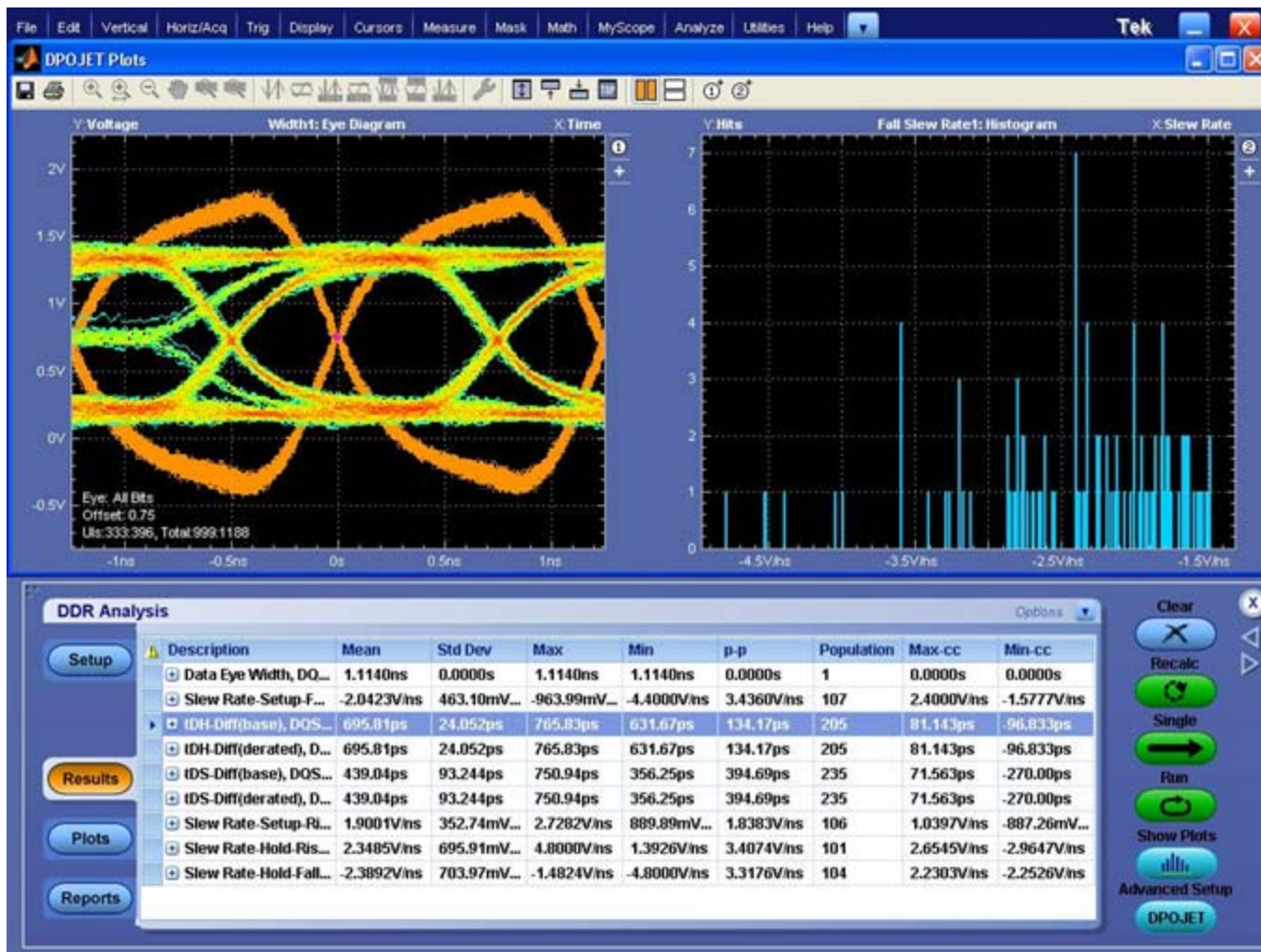
Challenge 5: Reporting and Archiving

- HTML Reports
- Source Waveforms



Challenge 6: Advanced Analysis and Debug

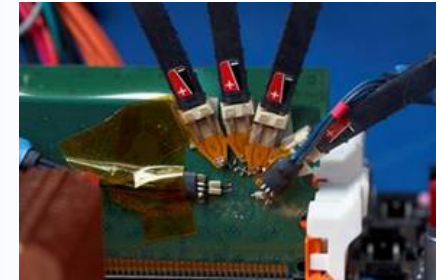
- DDRA has access to all plotting & debug tools in DPOJET



DDR Analog Validation & Debug – Tektronix Solutions

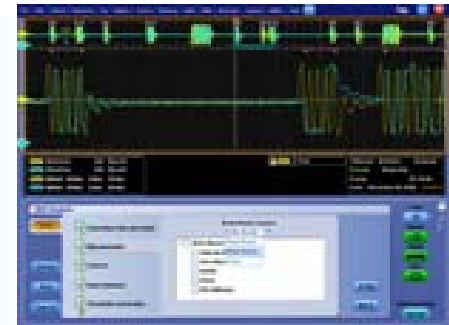
Signal Access - Probing

- P7500 TriMode Probing
 - Single probe for diff, CM and single-ended measurements
 - Up to 20 GHz bandwidth to the probe tip
- P6780 Logic Probe
 - 16 channel Active Differential probe with 2.5 GHz bandwidth
- Socketed BGA interposers for multiple exchanges



Signal Acquisition

- Automatically trigger and capture DDR signals
 - Identify and trigger directly on DQ, DQS in real-time to isolate Reads/Writes
 - Command Bus triggering with user-defined decode files
- Capture long time duration at high resolution
 - Direct connection to DPOJET for signal analysis
 - Time trend view for analysis of low frequency effects



Signal Analysis

- ▶ DDRA – Automated setup, read/write burst detection, JEDEC pass/fail meas.
- ▶ DPOJET – The most powerful Jitter, Eye and Timing analysis tool
 - Time, Amplitude, Histogram, measurements
 - Advanced Jitter, Eye diagram measurements and Pass/Fail testing
 - Many display and plotting options
 - Report generator

