

DDR Memory Bus Electrical Validation and Analysis Software



Features & Benefits

- Auto-configuration Wizard Guides Easy Setup and Test Configuration
- Analyze All Read/Write Bursts in the Entire Acquisition
- Plot DQS and DQ Eye Diagrams for Reads and Writes
- Perform JEDEC Conformance Tests with Pass/Fail Limits
- Use Chip Select to Qualify Multi-rank Measurements
- Navigate and Time Stamp Reads and Writes in an Acquired Record using Search and Mark
- Use Pinpoint Triggering and DPX to Quickly Identify Infrequent Anomalies
- Easily Move between Conformance-test and Analysis/Debug Tools
- Automatically Produce Consolidated Reports with Pass/Fail Information, Statistical Measurement Results, and Test-setup Information
- On MS070000, Use Address/Command Bus to Precisely Qualify Read and Write Bursts or Other Events

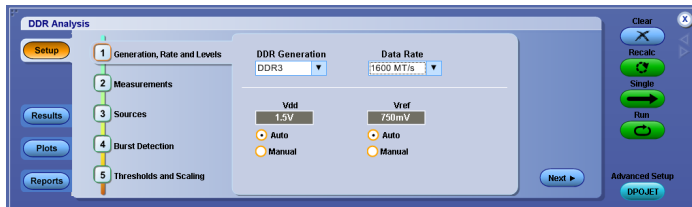
Applications

- DDR1
- DDR2
- DDR3
- GDDR3
- LPDDR
- LPDDR2

Option DDRA accelerates the analysis, validation, and JEDEC conformance testing of memory systems based on DDR1, DDR2, DDR3, and DDR derivative technologies like LPDDR, LPDDR2, and GDDR3. Option DDRA supports the common data rates plus custom data rates up to and beyond 2133 MT/s. Whether you are doing intensive signal integrity analysis or debugging a specific memory transaction, DDRA will speed your ability to trigger on and identify read and write bursts in the acquired data record and then perform parametric measurements on the signals of interest.

DDRA Wizard for Easy Test Selection and Configuration

The wizard consolidates Tektronix experience and expertise in DDR testing into a simple, easy-to-follow test selection interface. The user selects which DDR technology, speed grade, and measurement group (reads, writes, clocks, address, and control lines) they are testing, using check boxes to select some or all measurements in a category. DDRA can then automate oscilloscope scale selection, DQ and DQS level selections, and threshold detection, then automate burst identification using search and mark. Search and mark (for read/write measurements) data is used to identify and separate all read vs. write bursts across the entire acquisition and qualify measurement zones for use by DPOJET Advanced Jitter and Eye Analysis. DPOJET will generate an eye diagram of the data and perform JEDEC standard measurements qualified on read or write bursts. Measurement configurations and JEDEC pass/fail limits are automatically applied for the selected measurements. Every edge in each identified burst is measured, then measurement results are included in statistics and plots for a complete analysis of the acquired waveform.



DDR Analysis Menu

JEDEC-conforming Measurements and Conformance Testing

DDR Specification Conformance

DDR	JESD79E (May 2005)
DDR2	JESD79-2E (April 2008)
DDR3	JESD79-3D (September 2009)
LPDDR	JESD209A (February 2009)
LPDDR2	JESD209-2B (February 2010)

Comprehensive Measurements for JEDEC Conformance Testing

Option DDRA adds a long list of JEDEC-specific measurements to the rich toolset of generic jitter, timing, and signal-quality measurements already present in DPOJET. In addition to the measurements shown below (for DDR2 in this example), Option DDRA also performs de-rating of Setup and Hold pass/fail limits based on the result of slew rate measurements, as stipulated by JEDEC in the test specs for DDR2 and DDR3 (JESD79-3D, JESD79-2E as of this writing).

JEDEC Measurements Supported for DDR2

tCK (avg)	tDS - diff (base)	tIPW
tCK (abs)	tDS - SE (base)	tIS (base)
tCH (avg)	tDS - diff - DERATED	tIH (base)
tCH (abs)	tDS - SE - DERATED	tIS - DERATED
tCL (avg)	tDH - diff (base)	tIH - DERATED
tCL (abs)	tDH - SE (base)	Vid - diff (AC)
tHP	tDH - diff - DERATED	Vix (AC) - DQS
tJIT (duty)	tDH - SE - DERATED	Vix (AC) - CLK
tJIT (per)	tDIPW	Vox (AC) - DQS
tJIT (cc)	tAC - diff	Vox (AC) - CLK
tERR (02)	tDQSK - diff	InputSlew - Rise (DQS)
tERR (03)	tDQSK - SE	InputSlew - Fall (DQS)
tERR (04)	tDQSQ - diff	InputSlew - Rise (CLK)
tERR (05)	tDQSQ - SE	InputSlew - Fall (CLK)
tERR (6 - 10 per)	tQH	AC - Overshoot Amplitude - diff
tERR (11 - 50 per)	tDQSS	AC - Undershoot Amplitude - diff
tDQSH	tDSS	AC - Overshoot Amplitude - SE
tDQSL	tDSH	AC - Undershoot Amplitude - SE
		Data Eye Width

Easily Switch between Conformance Testing and Advanced Debug Tools

DDRA gives you the option to easily switch between conformance testing and advanced analysis and debug modes. The power of the DPOJET analysis engine allows you flexibility to reconfigure existing measurements or add new measurements not specifically required by JEDEC and to create new user-specified test limits. You can also use features like logging, filters, histograms, and time trends in addition to the information produced by the DDRA wizard.

Fast Fault Identification using Pinpoint® Triggers and DPX Technology

In addition to all of the measurement and analysis tools that DDRA offers, you can use Pinpoint® triggering and DPX® to find infrequent signal events. Pinpoint® triggering allows you to trigger on reads or writes so that all write bursts can be shown. Once you have set the hardware triggering on a read or write condition, you can use DPX®, the industry's highest waveform acquisition rate for signal integrity testing and to determine specific DDR read/write signal characteristics. DPX® enables quick identification of infrequent events by using a color-graded display to see both frequent and infrequent waveform events, such as areas where there is bus contention, reflections, or system timing issues.

Additional Capabilities using a Performance MSO (Mixed-Signal Oscilloscope)

The MSO70000 Series Performance MSOs allow you to probe more signals on the DDR bus and to trigger on and view specific bus events. Up to 16 digital channels can be used to view logic states of command and address signals such as RAS, CAS, WE, CE, CS, etc. Signal integrity of these 16 inputs can be analyzed using the iCapture™ multiplexing feature, which allows any of the digital input signals to be internally routed to one of the scope's four analog channels. Events such as initialization, power state changes, and command-bus cycle timing can also be analyzed using the bus-decoding features of the MSO.

Full Bus Analysis using Logic Analyzer and Oscilloscope

When full protocol analysis or probing of the entire memory bus is required, a logic analyzer can provide this additional capability. The TLA7000 Series logic analyzers can also be linked with Tektronix oscilloscopes to provide an integrated test setup using tools such as iCapture mentioned above. This eliminates the need for double probing and allows full analog capture of any signals probed by the logic analyzer. In addition, the iView™ display interface allows transfer of the oscilloscope data to the logic analyzer display, so that data from both instruments are analyzed and time-aligned on one display screen.

Characteristics

Bandwidth Recommendations for Each DDR Standard

DDR Type	Maximum Data Rate	Clock Rate	5th Harmonic of Clock	Max SE Slew Rate (JEDEC)	Typical Signal Swing	Oscilloscope Rise Time 10% - 90%*1	Recommended Oscilloscope BW*2
DDR	400 MT/s	200 MHz	1 GHz	5 V/ns	1.8 V	89 ps	4 GHz
DDR2	800 MT/s	400 MHz	2 GHz	5 V/ns	1.25 V	62 ps	6 GHz
DDR3	1600 MT/s	800 MHz	4 GHz	5 V/ns	1.0 V	49 ps	8 GHz

*1 For 3% maximum error on rise-time measurement.

*2 For less stringent applications, a one-step reduction in scope bandwidth may be acceptable.

Ordering Information

DDRA

DDR Memory Bus Electrical Validation and Analysis Oscilloscope Software.

To order on a new DPO7000, DPO7000B, DSA7000B*3, or MSO70000:

Order	Description
Opt. DDRA	Preinstall on a new DPO7000, DPO7000B, DSA7000B, or MSO70000 Series oscilloscope*4
DPOFL-DDRA	DDR Memory Technology Analysis Package – Floating License

*3 Note: Opt. DJA and ASM are standard on the DSA70000B Series oscilloscopes.

*4 Note: Opt. ASM (Advanced Event Search and Mark) and Opt. DJA (DPOJET) are required.

To upgrade an existing DPO7000, DPO7000B, DSA7000B, or MSO70000 order the appropriate model number and option listed below. For example, DPO7UP DDRA.

DPO7000	DPO7000B	DSA7000B	MSO70000
DPO7UP	DPO7UP	DPO7UP	DPO-UP

Upgrade options for DPO7000, DPO7000B, DSA7000B, MSO70000

DDRA	Upgrade to option DDRA (requires options ASM and DJA)
ASM	Upgrade DPO7000B and MSO70000 with Advanced Event Search and Mark (Opt. ASM)
DJAM	Upgrade DPO7000 with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DJAH	Upgrade DPO70404B - DPO70804B or MSO70404 - MSO70804 with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DJAU	Upgrade DPO71254B - DPO72004B or MSO71254 - MSO72004 with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)
DJUP	Upgrade DSA7000B with DPOJET Jitter and Eye Diagram Analysis (Opt. DJA)

Note: Software is supplied on the internal hard drive of the DPO/DSA7000B, MSO70000, and DPO7000 Series oscilloscopes. User documentation (online or user manual) is part of the oscilloscope documentation.

To order a floating license for an existing DPO7000, DPO7000B, DSA7000B, or MSO70000 use the orders listed below:

Order	Description
DPOFL-DDRA	DDR Memory Technology Analysis Package – Floating License
DPOFL-ASM	Advanced Event Search and Mark – Floating License
DPOFL-DJA	DPOJET Jitter and Eye Diagram Analysis – Floating License

Recommended Accessories

Order	Description
P7500 Series	TriMode™ Differential Probe
020-2955-xx	Micro-coax Tips (TriMode) for P7500 probes
020-3022-xx	Micro-coax Tips (TriMode) for P7500 probes*5
020-2954-xx	Socket Cable for P7500 probes
P6780	Differential Logic Probe for MSO70000

Recommended Nexus Technology Accessories

NEX-DDR3MP78BSC	BGA Interposer for DDR3 x4/x8-solder version
NEX-DDR3MP78BSCSK	BGA Interposer for DDR3 x4/x8-socket version
NEX-DDR3MP96BSC	BGA Interposer for DDR3 x16-solder version
NEX-DDR3MP96BSCSK	BGA Interposer for DDR3 x16-socket version
NEX-DDR2MP60BSC	BGA Interposer for DDR2 x4/x8-solder version
NEX-DDR2MP60BSCSK	BGA Interposer for DDR2 x4/x8-socket version
NEX-DDR2MP84BSC	BGA Interposer for DDR2 x16-solder version
NEX-DDR2MP84BSCSK	BGA Interposer for DDR2 x16-socket version

Note: For more detailed information contact <http://www.nexustechology.com>

*5 For use with BGA Interposers only.

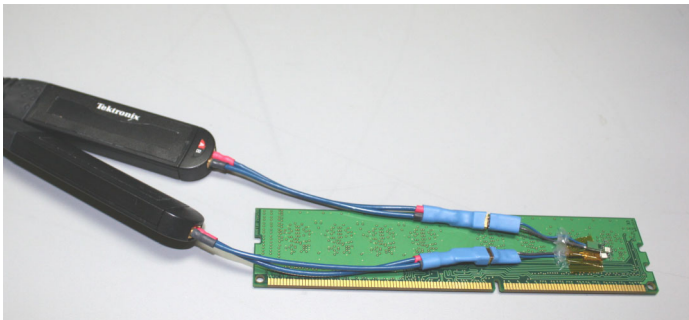


BGA Interposer probing solution for DDR2/DDR3

TLA7000 Series logic analyzer and Logic Probes Connection to the oscilloscope through Analog Mux. See www.tektronix.com/logic_analyzers



P7500 Series TriMode™ probe.



020-2955-xx Micro-Coax tips soldered to DIMM.



Product(s) are manufactured in ISO registered facilities.



Product(s) complies with IEEE Standard 488.1-1987, RS-232-C, and with Tektronix Standard Codes and Formats.

www.tektronix.com

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For Further Information. Tektronix maintains a comprehensive, constantly expanding collection of application notes, technical briefs and other resources to help engineers working on the cutting edge of technology. Please visit www.tektronix.com



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